Amendments to the Specification:

Please replace paragraph **[52]** with the following rewritten paragraph:

[52] Therefore, by fabricating the trace ~~T~~ C in Figure 8 from polysilicon, in the same polysilicon layer as the gate G, the prior art array of traces T in METAL 2 in Figure 3 has been eliminated. This elimination provides a thirty percent increase in space, due to factors which include the recovery of the space occupied by the traces T themselves. This elimination further provides a forty percent reduction in waste, by allowing packing of the type shown in Figure 12 to be attained, as opposed to that of Figure 11.